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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,019	12/07/2001	Francesco Pessolano	NL 000667	8972

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EXAMINER	
BUEHL, BRETT J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/020,019	PESSOLANO ET AL.	
	Examiner	Art Unit	
	Brett J Buehl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-11 and 13-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-11 and 13-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 5-11 and 13-15 have been examined. Claims 4 and 12 have been canceled by the Applicant.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: IDS as received on 05/10/02, Declaration and Fees as received on 02/25/02, Preliminary Amendment as received on 12/07/01, IDS as received on 12/07/01 and Foreign Priority Papers as received on 12/07/01.

Withdrawn Rejections

3. Applicant, via amendment, has overcome the 35 U.S.C. 102, 103 and 112 rejections set forth in the previous Office Action, except the 35 U.S.C. 112 rejection mentioned below. Consequently, the examiner has withdrawn these rejections.

Maintained Rejections

4. Applicant has failed to overcome the 35 U.S.C. 112 rejection for claim 15 as set forth in the previous Office Action. Therefore, these rejections are respectfully maintained by the examiner and copied below for applicant's convenience.

Maintained Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 15 recites the limitation, "Method according to claim 9", in the first line of the claim. There is insufficient antecedent basis for this limitation in the claim. The claim depends from an apparatus claim, which does not claim any method steps. The claim will be interpreted as reciting the limitation "Apparatus according to claim 9" for the purpose of this office action.

Claim Objections

8. Claims 2, 6-9, 11 and 13-14 recite the limitation "Apparatus according to" in line 1 of each claim. Please amend the claim language to read, "An apparatus according to" in order to be more grammatically correct.

9. Claim 5 recites the limitation "apparatus according to any one of claims 2" in line 1 of the claim. Please amend the claim language to read, "An apparatus according to claim 2" in order to be more grammatically correct.

NEW Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claim 7 recites the limitation, "wherein each stage is executed by a functional unit", in lines 2 and 3 of the claim. This limitation is indefinite, as it is unclear what "executing" a stage means. A functional unit typically executes an instruction. It is also unclear if "each stage" refers to each stage in the pipeline (i.e. fetch, decode, execute, commit and writeback) or just the execution stage. For the purposes of examination, the examiner will interpret this limitation to indicate the apparatus forms a pipeline with the functional units making up the execution stage.

NEW Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1-3, 5-11 and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by White et al., U.S. Patent No. 5,632,023, hereinafter referred to as White. It is noted that the "Intel Architecture Software Developer's Manual, Volume 2: Instruction Set Reference" is used to further explain teachings in White.

11. Regarding claim 1, White has taught a digital signal processing apparatus for executing a plurality of operations, comprising a plurality of functional units [235, 240, 245, 260 and 265 of Figure 2B] wherein each functional unit is adapted to execute operations [It is inherent that these

functional units execute operations], and control means for controlling said functional units, characterized in that said control means comprises a fetch unit [230 of Figure 2A], a decode unit [210 of Figure 2A], and a plurality of control units [235R, 240R, 245R, 260R and 265R of Figure 2B] responsive to said decode unit, wherein at least one control unit is operatively associated with a respective functional unit for controlling its function [Each reservation station receives decoded operations from the Decode Unit and issues the instructions to its associated functional unit when all operands are available (col. 11, lines 36-47), thereby controlling its function], and each functional unit is adapted to execute operations in an autonomous manner under control of the control unit associated therewith [Each and all of the functional units operate on a separate instruction under control of the reservation station associated thereto, meaning each and all of the functional units operate in an autonomous manner].

12. Regarding claim 2, White has taught an apparatus according to claim 1, characterized by FIFO (first-in/first-out) register means adapted for supporting data-flow communication among said functional units [285 of Figure 2A, the Reorder Buffer is a FIFO register (register meaning a device capable of retaining information of the aggregate information in a digital computer) device which is utilized by all of the functional units to support data-flow, in that the functional units can use the data before it is committed to the register file].

13. Regarding claim 3, White has taught a digital signal processing apparatus for executing a plurality of operations, comprising a plurality of functional units [235, 240, 245, 260 and 265 of Figure 2B] wherein each functional unit is adapted to execute operations [It is inherent that each functional unit is adapted to execute operations], and control means for controlling said functional units in coordination with one another [235R, 240R, 245R, 260R and 265R of Figure

2B, each reservation station receives decoded operations from the Decode Unit and issues the instructions to its associated functional unit when all operands are available (col. 11, lines 36-47), thereby controlling its function] in response to a single fetch unit [230 of Figure 2A] and a single decode unit [210 of Figure 2A], characterized by FIFO (first-in/first-out) register means adapted for supporting data-flow communication among said functional units [285 of Figure 2A, the Reorder Buffer is a FIFO register (register meaning a device capable of retaining information of the aggregate information in a digital computer) device which is utilized by all of the functional units to support data-flow, in that the functional units can use the data before it is committed to the register file].

14. Regarding claim 5, White has taught an apparatus according to claim 2, characterized in that said FIFO register means comprises a plurality of FIFO registers [285 of Figure 2A, the FIFO reorder buffer contains a plurality of entries, each being a FIFO register in that they are registers of the FIFO (register meaning a device capable of retaining information of the aggregate information in a digital computer)].

15. Regarding claim 6, White has taught an apparatus according to claim 1, characterized in that each of said functional units are provided with at least one control unit [235R, 240R, 245R, 260R and 265R of Figure 2B, each reservation station receives decoded operations from the Decode Unit and issues the instructions to its associated functional unit when all operands are available (col. 11, lines 36-47), thereby controlling its function].

16. Regarding claim 7, White has taught an apparatus according to claim 1, which apparatus is adapted to form a pipeline consisting of a plurality of stages, wherein each stage is executed by

a functional unit [The apparatus of White is a pipeline processor (superscalar pipeline), see Table 1, and the functional units form the execution stage, see Figures 2A&B].

17. Regarding claim 8, White has taught an apparatus according to claim 1, characterized in that for each control unit an instruction register and a counter are provided, wherein said counter indicates the number of times an instruction stored in said instruction register has to be executed by the corresponding functional unit [White has taught the use of the x86 instruction set on his processor (col. 9, lines 24-26), which includes the LOOP/LOOPcc instruction. The Intel Architecture Software Developer's Manual states "these instructions perform a loop operation using the ECX or CX register as a counter." (Page 3-372) Each functional unit has access to these registers, therefore each is provided with a counter. The instruction register is the reservation station of each functional unit, which holds the loop instruction while the ECX or CX register indicates the number of times to execute the instruction.].

18. Regarding claim 9, White has taught an apparatus according to claim 1, further comprising a program memory means storing a main program [302 of Figure 2B], characterized in that said main program contains directives for instructing said control units [It is inherent that the main program contains directives for instructing the control units].

19. Regarding claim 10, White has taught a method for processing digital signals in a digital signal processing apparatus, comprising a plurality of functional units [235, 240, 245, 260 and 265 of Figure 2B] wherein each functional unit is adapted to execute operations [It is inherent that the functional units execute operations], characterized in that said functional units are controlled by control means including a single fetch unit [230 of Figure 2A], a single decode unit [210 of Figure 2A] and a plurality of control units [235R, 240R, 245R, 260R and 265R of Figure

2B, each reservation station receives decoded operations from the Decode Unit and issues the instructions to its associated functional unit when all operands are available (col. 11, lines 36-47), thereby controlling its function] wherein at least one control unit is operatively associated with a respective unit [Each and all of the functional units have a reservation station] so that each functional unit is able to execute operations in an autonomous manner under control of the control unit associated therewith [Each and all of the functional units operate on a separate instruction under control of the reservation station associated thereto, meaning each and all of the functional units operate in an autonomous manner].

20. Regarding claim 11, White has taught an apparatus according to claim 9, characterized in that data-flow communication among said functional units is supported by FIFO (first-in/first-out) register means [285 of Figure 2A, the Reorder Buffer is a FIFO register (register meaning a device capable of retaining information of the aggregate information in a digital computer) device which is utilized by all of the functional units to support data-flow, in that the functional units can use the data before it is committed to the register file].

21. Regarding claim 13, White has taught an apparatus according to claim 10, wherein a pipeline consisting of a plurality of stages is provided, and each stage is executed by a functional unit [The apparatus of White is a pipeline processor (superscalar pipeline), see Table 1, and the functional units form the execution stage, see Figures 2A&B].

22. Regarding claim 14, White has taught an apparatus according to claim 10, characterized in that the number of times an instruction stored has to be executed by a functional unit is counted by the corresponding control unit [White has taught the use of the x86 instruction set on his processor (col. 9, lines 24-26), which includes the LOOP/LOOPcc instruction. The Intel

Architecture Software Developer's Manual states "these instructions perform a loop operation using the ECX or CX register as a counter." (Page 3-372) Each functional unit has access to these registers, therefore each is provided with a counter. The instruction register is the reservation station of each functional unit, which holds the loop instruction while the ECX or CX register indicates the number of times to execute the instruction. The functional unit control counts the number of times the instruction executes in that it issues the instruction following the LOOP instruction when the count is gets to zero.]

23. Regarding claim 15, White has taught an apparatus according to claim 9, wherein a main program is stored in a program memory means [302 of Figure 2B], characterized in that said main program contains directives for instructing said control units [It is inherent that the main program contains directives for instruction said control units].

Response to Remarks

24. Applicant's arguments with respect to claims 1, 3 and 10 have been considered but are moot in view of the new ground(s) of rejection. The amended claim 1 narrows the limitations of the original claim 1 by limiting the apparatus to having a fetch unit, a decode unit and a plurality of control units responsive to said decode unit. The amended claim 3 narrows the limitations of the original claim 3 by limiting the apparatus to having a single fetch unit and a single decode unit. The amended claim 10 narrows the limitations of the original claim 10 by limiting the method to having a single fetch unit and a single decode unit. These limitations were not found in any previous claim in the original filing and therefore the scope of claims 1-3, 5-11 and 13-15 has changed.

25. It is noted that the Applicant stated in his arguments that claims 4 and 13 were cancelled. However, the amended claims show claim 12 as cancelled and claim 13 as amended. The examiner has taken the amended claims as the intended cancellation.

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

27. Inquiries concerning this communication or earlier communications from the examiner should be directed to Brett J. Buehl who can be reached at (703) 305-4663. The examiner can normally be reached between the hours 8:00am – 5:30pm (EST), Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan, can be reached at (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

28. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brett J. Buehl
Patent Examiner
Art Unit 2183